1. Course Number and Name: 414CPE – Integrated Circuit Design

2. Credits and Contact Hours: 3 Credit

a.Lecture – 2 day per week at 50 minutes for 16 weeks
b.Laboratory – 1 day per week at 100 minutes for 16 weeks

3.Course Coordinator or Instructor:

Dr.JamelBaili

4. Text Book:

- CMOS Digital Integrated Circuit Design, Sung Mo-Kang, Yusuf Leblebici , 2nd Edition, McGraw-Hill.
- Introduction to Digital Systems: Modeling, Synthesis, and Simulation Using VHDL, Mohammed Ferdjallah, Wiley, 2011.

5. Specific Course Information:

a. **Catalog Description:**Students will study Integrated Circuits Design Principles including VLSI and parallel processing principles.
b. **Prerequisites:**CPE324 Computer interfacing circuits c. **Status:** Required

6.Specific Goals for the Course:

a.Course Outcomes:

1.Define the fundamental principles of integrated circuits design
2.Describe the recent trends and current job market in the field of IC Design.
3.Develop an ability to design an integrated circuits, components to meet desired needs within realistic constraints
4.Explain key impact of integrated circuits design solutions in a global, economic and societal context.
5.Explain the techniques, skills and tools necessary for integrated circuits design practice
6.Use the discussion and participation during the lectures to better knowledge of technological skills for integrated circuits design.
7.Demonstrate and ability to think analytically and critically to design an integrated circuits.

b.Student outcomes in Criterion 3 addressed by course:

Course LOs #	Map course LOs with the program LOs. (Place course LO #s in the left column and Student LO #s across the top.) Student Learning Outcomes Use LOs Codes											
	a1	a2	b1	b2	b3	b4	c1	c2	c3	c4	d1	d2
1	√											
2		√										
3				√								
4						√						
5							√					
6								√				
7										√		

7. List of Topics: 414CPE – Integrated Circuit Design

List of Topics for Theory:

- **Introduction to IC Design:** Introduction, Historical perspective, VLSI Design methodologies, VLSI Design Flow, Design Hierarchy, Design Styles, Design Quality, CAD Technology.
- **Fabrication of MOSFETs:** Fabrication process, NMOS Fabrication, CMOS n-well process, Layout Design rules, Stick Diagrams, Layout Design, Design rules.
- **Basic of VHDL language:** Introduction to VHDL language, Basic Form of VHDL Code, Modeling Styles, Entity, Architectures, Process, Package, Components declaration, Parallel expressions (if, case wait and loops), Components instantiation, Examples.
- **MOS Transistor:** Review of Structure and operation of MOSFET (n-MOS enhancement type), CMOS, MOSFET V-I characteristics, MOSFET scaling and small geometry effects, MOSFET capacitance.
- **MOS Inverters:** Static Characteristics & Switching Characteristics - Basic NMOS inverter, characteristics, inverters with resistive load and with n-type MOSFET load, CMOS inverter and characteristics. Delay time definitions and calculations, inverter design with delay constraints, estimation of parasitic switching power dissipation of CMOS inverters.
- **Combinational & Sequential MOS logic circuits:** CMOS logic circuits, complex logic circuits, pass transistor logic, sequential logic circuit – introduction, SR latch, clocked latch and flip-flop circuits, CMOS D latch and edge triggered flip-flop.
- **Dynamic logic circuits:** Dynamic logic, basic principles, Dynamic RAM, SRAM, flash memory.

List of Topics for Laboratory:

- Introduction to VHDL language & Xilinx ISE environment.
- Program to simulate a Half Adder using 1.Data flow Model. 2. Behavioral Model. Generate a synthesis report and generate bit file (bit stream).
- Program to simulate a Full Adder using 1.Data flow Model. 2. Behavioral Model and generate a synthesis report.
- Program to simulate a 8x1 Multiplexer using Behavioral model generate a synthesis report
- Program to simulate a 1x8 De-multiplexer using data flow model generate a synthesis report
- Program to simulate a 8x3 Encoder using data flow model generate a synthesis report
- Program to simulate a 3x8 Decoder using data flow model generate a synthesis report
- Program to simulate a J-K Flip-flops using data flow model generate a synthesis report/Home Work
- Program to simulate D,T Flip-Flops using data flow model generate a synthesis report
- Program to simulate a Up-down Counter using data flow model generate a synthesis report
- Program to simulate a BCD to 7-Seg Decoder using data flow model generate a synthesis report
- Program to simulate a Mealy state machine using Behavioral model and generate a synthesis report.